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transmission can be improved by the shortening of the I/O slot wiring. The improvement of the delay in the signal transmission will now be described.

On page 12, replace the paragraph beginning on line 2 with the following:

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Incidentally, the I/O slot to be replaced is not limited to the adjacent slot. For example, the rewiring 24, 33 as shown in FIG. 1 can be extended to reach the wiring in the outermost peripheral area such as the I/O slots 11c and 11d. It is also possible to interchange the I/O slots apart from each other by at least two slots.

IN THE CLAIMS:

Please cancel claims 2 and 3 without prejudice or disclaimer of the subject matter thereof, amend claim 1, and add new claims 4-14, as follows:

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1. (Amended) A semiconductor integrated circuit device, comprising:

first and second I/O slots arranged in parallel along a peripheral portion of a chip within an inner region of the chip and connected to input/output cells of the chip;

a first pad arranged above said first I/O slot;

a second pad arranged above the first I/O slot and a predetermined distance apart from the first pad in a direction extending from the peripheral portion of the chip toward a central portion;

a first wiring having one end positioned in said first pad and having the other end positioned in the peripheral portion of the inner region of the chip above the first I/O slot;

a second wiring having one end positioned in the second pad and having the other end positioned in the peripheral portion of the inner region of the chip above the second I/O slot;

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a third wiring arranged in an outermost peripheral portion of the chip and serving to connect the other end of the first wiring to the second I/O slot, the third wiring being isolated from the second wiring; and

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a fourth wiring arranged in the outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot, the fourth wiring being isolated from the first wiring.

Please add the following new claims:

4. (New) The semiconductor integrated circuit device according to claim 1, wherein the third wiring and the fourth wiring do not overlap.

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5. (New) The semiconductor integrated circuit device according to claim 1, wherein the fourth wiring is shorter than the third wiring.

6. (New) The semiconductor integrated circuit device according to claim 1, wherein the first and second I/O slots, the first and second pads and the first wiring and the second wiring are each designed and fixed in advance.

7. (New) The semiconductor integrated circuit device according to claim 1, wherein the first wiring and the second wiring are the same in wiring level.

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8. (New) The semiconductor integrated circuit device according to claim 1, wherein the first wiring and the second wiring are arranged in an uppermost layer of the chip.

9. (New) A semiconductor integrated circuit device, comprising:

first and second I/O slots arranged in parallel along a peripheral portion of a chip within an inner region of the chip and connected to input/output cells of the chip;

a first pad arranged above the first I/O slot:

a second pad arranged above the first I/O slot and a predetermined distance apart from the first pad in a direction extending from the peripheral portion of the chip toward a central portion;

a first wiring having one end positioned in the first pad and having the other end positioned in the peripheral portion of the inner region of the chip above the first I/O slot;

a second wiring having one end positioned in said second pad and having the other end positioned in the peripheral portion of the inner region of the chip above the second I/O slot;

a third wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the first wiring to the second I/O slot; and

a fourth wiring arranged in the outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot, the fourth wiring being shorter than the third wiring.

SUB B2

A5 CONT.

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SUB B2

10. (New) The semiconductor integrated circuit device according to claim 7, wherein the third wiring is isolated from the second wiring, and the fourth wiring is isolated from the first wiring.

11. (New) The semiconductor integrated circuit device according to claim 7, wherein the third wiring and the fourth wiring do not overlap.

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12. (New) The semiconductor integrated circuit device according to claim 7, wherein the first and second I/O slots, the first and second pads and the first and second wiring are each designed and fixed in advance.

13. (New) The semiconductor integrated circuit device according to claim 7, wherein the first wiring and the second wiring are the same in wiring level.

14. (New) The semiconductor integrated circuit device according to claim 7, wherein the first wiring and the second wiring are arranged in an uppermost layer of the chip.

IN THE DRAWINGS:

Subject to the approval of the Examiner, please amend Fig. 4 by including the legend "Prior Art", as proposed in the accompanying "Request for Approval of Drawing Change" filed herewith.

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